High Capacitance Damascene Capacitors

FIELD OF THE INVENTION

The invention is generally related to the field of semiconductor devices and fabrication and more specifically to high capacitance damascene capacitors.

BACKGROUND OF THE INVENTION

Capacitors built into the backend interconnect structures are useful in some circuits. Currently there are a number of schemes for fabricating such capacitors using aluminum based interconnect technology. Here, silicon dioxide is used to form the isolation layers between the various aluminum metal layers in the integrated circuit. With a dielectric constant of about 3.9 silicon dioxide is a suitable capacitor dielectric. Current schemes involve using the various metal levels as the plates of the capacitor structures. Such a capacitor is shown in Figure 1. In the Figure, silicon dioxide layers 12, 14, 16, 18, on the silicon substrate 10 represent the isolation layers between the various aluminum metal layers 22. Alternate metal layers 22 are connected using vias 24 to increase the capacitance of the structure.

The requirement of higher clock rates has lead to the use of copper to form the metal interconnect lines in integrated circuits. In addition to the use of copper, isolation layers such as florosilicate glass (FSG) (dielectric constant ~3.6) and organosilicate glass (OSG) (dielectric constant ~2.6) are currently being used to take advantage of the lower dielectric constant of such materials compared to silicon dioxide. To achieve the same capacitance value using a dielectric with a lower dielectric constant, capacitors with larger areas have to be formed. This increased area requirement is in direct contrast to the requirement of higher integration and reduced area devices. In integrated circuits using copper interconnect lines, there is a need for a high capacitance structure with reduced area.

SUMMARY OF THE INVENTION

The present invention describes a high capacitance damascene capacitor and a method for making the same. The capacitor comprises: a first conductive layer with a top surface; a second conductive layer with a bottom surface; and a dielectric layer adjacent to said top surface of said first metal layer and to said bottom surface of said second metal layer.

In addition to the above described capacitor structure, the first conductive layer is copper, the second conductive layer is a material selected from the group consisting of aluminum, aluminum oxide, tantalum nitride, titanium nitride, tungsten, tungsten nitride, silicon carbide, and their alloys, and the dielectric layer is silicon nitride.

A method of making the high capacitance damascene capacitor according to the instant invention comprises: providing a silicon substrate with a first dielectric film containing at least one copper layer; forming a second dielectric layer over said first dielectric layer and said copper layer; forming a first conductive layer over said first dielectric layer; and removing a region of said first conductive layer such that a portion of said second dielectric layer remains between said first conductive layer and said copper layer. The above described method further comprises: forming copper contacts to said first conductive layer; and forming a second copper layer that electrically contacts said copper contacts. In addition to the above, the second dielectric layer is an etch-stop/barrier layer.

BRIEF DESCRIPTION OF THE DRAWINGS

In the drawings:

FIGURE 1 is a cross-sectional diagram of a stacked aluminum capacitor.

FIGURES 2A-2F are cross-sectional diagrams illustrating one embodiment of the instant invention.

FIGURE 3 is a cross-section diagram illustrating a stacked capacitor scheme according to an embodiment of the instant invention.

DETAILED DESCRIPTION OF THE INVENTION

The invention will now be described with reference to Figures 2A - 2F and Figure 3. It will be apparent to those of ordinary skill in the art that the benefits of the invention can be applied to other structures where high value capacitor is required.

A silicon substrate 100 may be single-crystal silicon or an epitaxial silicon layer formed on a single crystal substrate is shown in Figure 1. This substrate may contain any number of integrated circuit devices such as transistors, diodes, etc., which all form part of the integrated circuit. This devices are omitted from Figures 2A - 2F for clarity. Following the fabrication of such devices, a first intra-metal-dielectric (IMD) layer 30 is formed on the substrate and copper metal layers 40 and 50 are formed in the IMD layer 30. Typically, these copper layers 40, 50 are formed using a damascene process. In the damascene process a trench is first formed in the IMD layer 30. A trench liner/barrier film is then formed in the trench followed by copper deposition. The trench liner usually comprises a tantalum nitride film with typical field thickness on the order of 100A - 2000A. Following

copper film formation, which completely fills the trench, chemical mechanical polishing (CMP) is performed to remove the excess copper and produce the copper layers 40 and 50 whose top surfaces are planar with the surface of the IMD layer 30 as shown in Figure 2A. The copper layer 40 will function as one plate of a capacitor structure and 50 is part of the metal interconnect structure associated with a metal level or layer in the integrated circuit.

Following the formation of the copper layers 40 and 50, a dielectric film 60 is formed on the top surface of the IMD layer 30 and the copper layers 40 and 50. In an embodiment of the instant invention, this dielectric film comprises silicon nitride with typical thickness of 50A - 500A. In typical integrated circuit copper processes this dielectric film functions as a etch-stop and barrier layer. However in regions where capacitors are to be formed, this dielectric film will function as the capacitor dielectric. Such a region 65 is shown in Figure 2B. In addition to silicon nitride, any other dielectric film which can function as a capacitor dielectric can be used. In addition to single dielectric films, alternating layers of different dielectric films can be used to form this layer 60.

Following the formation of the dielectric layer 60, a conductive layer 70 is formed on the dielectric layer 60, as shown in Figure 2(c). This conductive layer 70 can be any conductive material, including organic conductors, which is easily integrated into integrated circuit processing. In an embodiment of the instant invention this conductive layer 70 is approximately 50A to 300A thick and is formed using a material from the group consisting of aluminum, aluminum oxide, tantalum nitride, titanium nitride, tungsten, tungsten nitride, silicon carbide, and their alloys. The key characteristics of the material used to form the conductive layer 70 are: it is conductive (including semiconductive, which can be heated to make conductive), and it has etch selectivity against the dielectric layer which is formed above it. Some conductive polymers may not meet the above criterion.

Following the formation of the conductive layer 70, a photoresist film is formed and patterned 72 on the conductive film 70 over the region 65 where the capacitor is to be formed. This patterned photoresist film 72 will protect the underlying conductive film 70 during the subsequent etch process to remove unprotected regions of the conductive film 70. The patterning process is not

restricted to photolithography and the use of photoresist. Additional techniques such as e-beam lithography could also be used to pattern the film. The conductive film 70 is selectively etched and the patterning film 72 is removed.

As shown in Figure 2D, the portion of the conductive film 75 which remains after the etch process will function as a plate of the capacitor. For the capacitor structure shown in Figure 2D, the copper layer 40 and the patterned conductive film 75 both function as plates of the capacitor and that portion of the dielectric layer 65 which lies between 40 and 75 functions as the capacitor dielectric. The large capacitance values of the capacitor formed from 75, 65, and 40 is due to the thin dielectric layer 60 which has a high dielectric constant compared to that of commonly used dielectric materials such as silicon dioxide, FSG, and organosilicate glass (OSG). Following the formation of the patterned conductive film 75, an inter layer dielectric (ILD) 80 is formed on the structure. In an embodiment of the instant invention this ILD layer 80 comprises a conventional silicon oxide layer, a FSG layer or a OSG layer that is about 2000A - 7000A thick. A planarization step may be necessary after the ILD deposition. An etch-stop layer 90 is then formed on the ILD layer. In an

embodiment, this etch stop layer 90 comprises a 50A - 600A thick silicon nitride film. A 3000A - 5000A thick IMD layer 100 is then formed on the etch-stop layer 90 which can be comprised of silicon oxide, FSG, OSG or any material with similar properties. It should be noted that in other embodiments of the instant invention the etch-stop layer 90 can be omitted without changing the scope of the invention. In the case where this etch-stop layer 90 is omitted, the ILD and IMD material may be identical and homogeneous. Following the formation of the ILD/etch-stop/IMD stack 80/90/100, openings for vias 73 are formed using standard photolithographic patterning followed by etching processes. The etching processes will comprise an IMD etch for 100 followed by an etch-stop etch for 90 followed by an ILD etch for 80. A criteria of the ILD etch process is that it be selective with respect to the etch-stop/barrier material 60 and also to the patterned conductive film 75.

Following the formation of the via openings 73, a protective film 110 is formed on the structure as shown in Figure 2E. In an embodiment of the instant invention, this protective film comprises an anti-reflective coating or a BARC film. This film 110 partially fills the via openings 73 and will protect the material at the bottom of the via

openings 73 during the subsequent trench etch process. A photoresist film is then formed and patterned 120 on this protective coating 110 to define the regions of the IMD layer 90 that will be removed during the trench etch process. In forming the trenches in the IMD layer 100, the layer is first etched with an etch process that is selective with respect to the etch barrier 90. This selective etch process removes those portions of the IMD layer 100 not protected by the patterned photoresist film 120. In addition, this etch process also removes the BARC film 100 from the via openings 73. Following this IMD etch, a blanket etch process is performed that removes any etch-stop material remaining at the bottom of the via openings 73. Because the patterned conductive film 75 will be exposed to this etch process it is important that this etch process be selective to the material of the patterned conductive film 75. Following the removal of the remaining photoresist 120, a trench liner film is formed on the structure followed by the deposition of a copper layer that completely fills the vias and the trenches on the structure. The trench liner usually comprises a tantalum nitride film with typical thickness on the order of 50A - 300A. CMP processes are used to remove any excess copper resulting in the structure shown in Figure 2F. The copper

structure 130 provides electrical contact to the patterned conductive film (i.e. capacitor plate) 75 and the copper structure 132 functions as part of the metal interconnect of the integrated circuit.

The capacitor structure is formed by the copper layer 40, the dielectric (etch-stop) layer 65, and the conductive film 75. Layer 60 serves the dual purpose of acting as the capacitor dielectric 65 and a etch-stop/barrier layer for other areas of the integrated circuit. The formation of the conductive film 75 is added to the integrated circuit processing sequence to form a plate of the capacitor. Following the formation of the capacitor structure, any number of different schemes can be used to contact the plates of the capacitor. The embodiment described above represents one such scheme. In addition, any number of such capacitors can be connected in parallel to increase the value of capacitance. Various shapes can be used to form the capacitor plates 40 and 75 to increase the capacitance including an inter-digitated scheme. Such a scheme comprises a series of interlocking fingers formed by the capacitor plates.

Shown in Figure 3 is a stacked capacitor structure according to an embodiment of the instant invention. Region 220 of the etch-stop/barrier dielectric layer 60 forms the dielectric region between the copper layer 40 and the conductive layer 75 which form the plates of a capacitor. A second dielectric layer is formed above the conductive layer 75 and a second copper layer 140 is formed in this dielectric layer. A second dielectric etch-stop/barrier layer 150 is formed and a second conductive layer 160 is formed above this dielectric etch-stop/barrier layer. Region 230 of the second etch-stop/barrier layer 150 functions as the capacitor dielectric. A third dielectric layer 180 is formed above the second conductive layer 160 and a third copper layer 190 is formed in this dielectric layer 180. A third dielectric etch-stop/barrier layer 200 is formed and a third conductive layer 210 is formed on this dielectric etch-stop/barrier layer 200. All the conductive layers 75, 160, and 210 can be formed using a material from the group comprising aluminum, aluminum oxide, tantalum nitride, titanium nitride, tungsten, tungsten nitride, silicon carbide, and their alloys. To form the stacked capacitor structure a first set of vias 220 are used to electrically connect all the existing conductive layers 210, 160, and 75 and a second set of vias

230 are used to electrically connect all the copper layers 40, 140, and 190. This stacked capacitor structure can be extended to any number of copper layer and conductive layer capacitors. The above described method of interconnecting the various capacitors is one embodiment of the instant invention. Any parallel connection of the various capacitors can be used to produce a stacked capacitor structure according to the instant invention.

While this invention has been described with reference to illustrative embodiments, this description is not intended to be construed in a limiting sense. Various modifications and combinations of the illustrative embodiments, as well as other embodiments of the invention will be apparent to persons skilled in the art upon reference to the description. It is therefore intended that the appended claims encompass any such modifications or embodiments.